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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,001	11/20/2003	Alexander J. Eglit	GENSP103R1	3976

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EXAMINER	
LAO, LUN YI	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,001	EGLIT, ALEXANDER J.	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-115* is/are pending in the application.

4a) Of the above claim(s) *26-115* is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12-18 and 20* is/are rejected.

7)☐ Claim(s) *19 and 21-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/25/2005, 10/4/2004, 7/26/2004, 6/18/2004, 6/8/2004, 6/2/2004 and 11/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reissue Applications

1. The person who signed the submission establishing ownership interest is not recognized as an officer of the assignee, and he/she has not been established as being authorized to act on behalf of the assignee. See MPEP § 324.

The signature of a general counsel is not acceptable since the person as an officer of the assignee is not presumed to have authority to sign the submission on behalf of the assignee.

2. This application is objected to under 37 CFR 1.172(a) as lacking the written consent of all assignees owning an undivided interest in the patent. The consent of the assignee must be in compliance with 37 CFR 1.172. See MPEP § 1410.01.

A proper assent of the assignee in compliance with 37 CFR 1.172 and 3.73 is required in reply to this Office action.

Election/Restrictions

3. Applicant's election with traverse of Group I(claims 1-25) in the reply filed on 3/29/2006 and 2/24/2006 is acknowledged. The traversal is on the ground(s) that Group I should be classified to class 345, subclass 698 that is the classification ascribed to Group II(claims 26-43). This is not found persuasive because Group I(claims 1-25) is

directed to a clock circuit in a digital display unit for recovering a time reference signal associated with analog display data, classified in class 345, subclass 213 and Group II(claims 26-43) is directed to a method for scaling a source image and provide designation image in accordance with a destination frame rate , classified in class 345, subclass 698. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper. The new claims 106-114 should belong to Group II of a method for scaling a source image and new claim 115 should belong to Group III of a memory display controller comprising a line buffer.

The requirement is still deemed proper and is therefore made FINAL.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters number "223" and "234" cited on column 3, lines 9-20 of the US Patent No. 6,320,574 are not showed in the drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The Serial Numbers of 11/408,528 and 11/408,669 should be inserted in the amendment for the Specification filed on March 9, 2006.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 13 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The recitation of "an analog filter to eliminate any undesirable frequencies said signal representative of said sampling clock to generate said sampling clock" in claim 13 is unclear since the analog filter(320) for eliminate a signal output from the digital

circuit(310), not the sampling clock signal generated from the clock generator(e.g. 300)(see figure 3).

The recitation of "said sampling clock has a sampling frequency equal to said time reference signal frequency" in claim 18 has not been disclosed by the specification. The specification only disclose the sampling clock is designed to have a frequency such that the display portion of each horizontal scan line is sampled a desired number of times(see column 2, lines 36-46 of the US patent No. 6,320,574); and the sampling clock synchronized with the time reference(REF) and the output signal from the analog filter(320) is divided by K, where K corresponds to the number of samples taken per each horizontal source image line(see figure 3 and column 5, lines 26-33 of the US patent No. 6,320,574).

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 17 is recites the limitation of "said reference clock" in claim 17, line 1. lacks an antecedent basis since it is unknown "said reference clock" is the clock generator or the time reference signal.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 12, 14, 16-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada(6,078317) in view of Murata et al(6,144,355).

As to claims 12, 14, 16-18 and 20, Sawada teaches a circuit for use with a digital display unit(FLCD) for generating a plurality of digital image data elements from analog image data(input from a computer 12) received by the digital display unit(FLCD)(see figure 1; column 1, lines 63-68; column 2, lines 1-16; column 3, lines 61-65; column 5, lines 61-68 and column 6, lines 1-6), wherein the digital display unit(FLCD) further receives a time reference signal(Horizontal Synchronizing Signal) having a time reference signal frequency associated with the analog image data(see figures 1-2; column 3, lines 38-65 and column 4, lines 61-66). Sawada teaches the circuit comprising an analog-to-digital converter(A/D converter, 13) for sampling the analog image data using a sampling clock(41) to generate the plurality of digital image data elements(see figures 1-2; column 3, lines 38-68 and column 4, line 1); a clock generator circuit(14) for generating the sampling clock(41) that is synchronized with the time reference signal(Horizontal Synchronizing Signal) and a circuit for receiving the time reference signal(Horizontal Synchronizing Signal) and a feedback signal, wherein the feedback signal is generated by dividing the sampling clock(41)(see figures 1-2; column 4, lines 61-68 and column 5, lines 1-12).

Sawada fails to disclose a digital circuit or digital phase-locked loop circuit.

Murata et al teach a circuit comprising a digital circuit(see figure 10) for receiving time reference signal(SCK) and a feedback signal, wherein the feedback signal is generated by dividing the sampling clock(SCK'), the digital circuit generating the digital input according to the difference of the phase of the phase of the time reference signal and the feedback signal(see figures 1, 10, 13-14 and column 8, lines 16-24). It would have been obvious to have modified Sawada with the teaching of Murata et al, since Murata et al have disclose an analog phase-locked loop circuit could replaced by phase-locked loop circuit(see figures 9-10; column 7, lines 64-68; column 8, lines 1-24); and an analog phase-locked loop circuit could replaced by phase-locked loop circuit could lower the jitter cutoff frequency(see column 7, lines 64-68 and column 8, lines 1-7) and provide an excellent, high-quality/high-precision display images even in extra-high speed operation(see column 8, lines 40-44).

As to claim 14, Sawada as modified teach a phase and frequency detector(32) for determining the difference of phase between the feedback signal and the time reference signal(see figure 2 and column 4, lines 60-66).

As to claim 16, Sawada as modified teach the analog image data and the time reference signal are received on two separate signal paths(11, 12)(see figures 1-2 and column 3, lines 38-60).

As to claim 17, Sawada teaches a clock generator having a binary signal(Dot Clock Signal)(see figures 1-3).

As to claim 18, it would have been obvious to have a sampling frequency equal to the time reference signal frequency since the sampling frequency is depend on how many pixels are sampling in a horizontal line(see Sawada's figures 1-3).

As to claim 20, Sawada as modified teach a digital display comprising a display screen(4) and a panel interface arranged to generate display signals for the display screen(4) based on the plurality of digital image data elements(see figures 1-3; column 1, lines 64-68; column 2, lines 1-21; column 3, lines 37-68 and column 4, lines 1-9).

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada(6,078317) in view of Murata et al(6,144,355) and Lablebicioglu(5,369,376).

Sawada as modified fail to disclose a charge/discharge control logic.

Lablebicioglu teaches a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of the difference of phase(phase error)(see figures 7-9B; column 11, lines 65-68 and column 12, lines 1-19). It would have been obvious to have modified Sawada as modified with the teaching of Lablebicioglu, so as to provide a programmable phase locked loop circuit having transfer function characteristics that can be selectively programmed without switching resistive and/or capacitive elements within the loop filter(see column 3, lines 46-47).

Allowable Subject Matter

13. Claims 1-11 are allowable.

14. Claims 19 and 21-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Powell(5,790,614) teaches an analog PLL(see figure 2) and a digital PLL(see figure 3).

Kato et al(4,906,941) teach a digital phase locked loop circuit.

Shiki(5,406,308) teaches an LCD display having a PLL circuit(7).

Nakamura(6,046,737) teaches an LCD display having a PLL circuit(see figure 5),

Parrish et al(5,638,131) teach a display system having a PLL circuit.

Kim(5,528,305) teach a display system having a clock generator.

Kurikko(5,841,430) teaches a display having a PLL circuit(35).

Yamano et al(5,535,018) a display having a PLL circuit(105).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 23, 2006

Lun-yi Lao
Primary Examiner